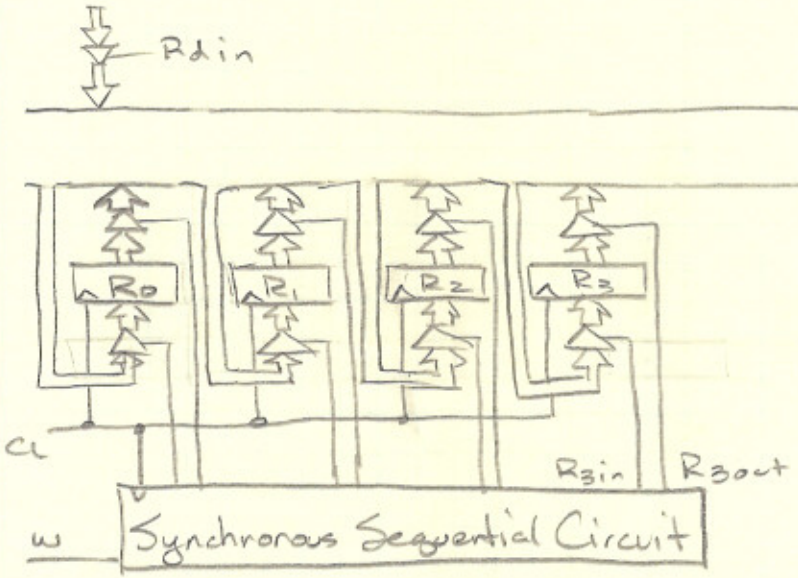
Digital System Design



We want to exchange the information from R_0 & R_3

$$[R_0] \rightarrow R_3$$
$$[R_3] \rightarrow R_0$$

The information in R_1 & R_2 is not important, we need these registers to perform this opperation.

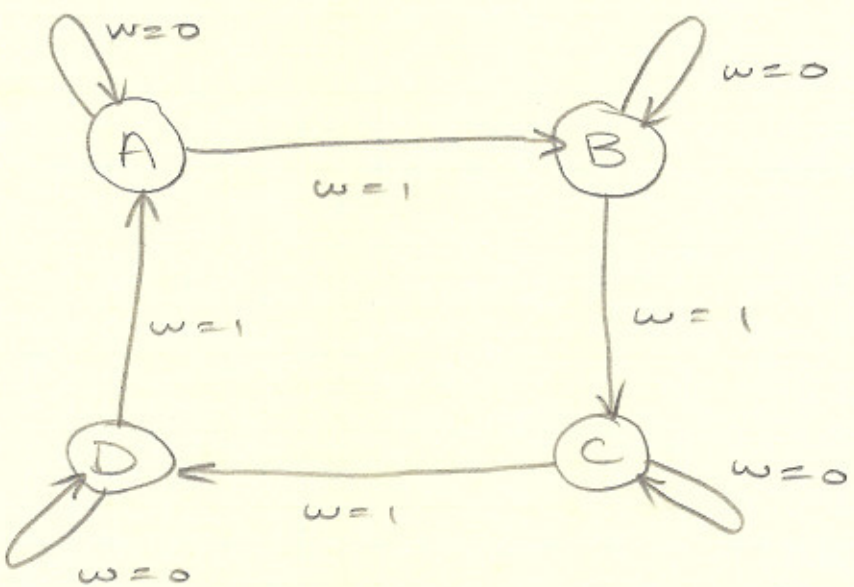
Steps

* $[R_0] \rightarrow R_1$
* $[R_3] \rightarrow R_0$
* $[R_1] \rightarrow R_3$

We also will need a null state :.

State		
A		
B	$R_{0out} = 1$	$R_{1in} = 1$
C	$R_{3out} = 1$	$R_{0in} = 1$
D	$R_{1out} = 1$	$R_{3in} = 1$

State Diagram (1)



State table (2)

Current State	Next State w=0	Next State w=1	Output state
A	A	B	Z_0
B	B	C	Z_1
C	C	D	Z_2
D	D	A	Z_3

State Assignment (3)

	$y_1 y_0$
A	00
B	01
C	10
D	11

State Assignment Process (4)

Current State		Next State w=1		Next State w=0		Outputs In				Outputs Out			
y_1	y_0	y_1	y_0	y_1	y_0	R_0	R_1	R_2	R_3	R_0	R_1	R_2	R_3
0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	1	0	1	0	0	1	0	0	0
1	0	1	1	1	0	1	0	0	0	0	0	0	1
1	1	0	0	1	1	0	0	0	1	0	1	0	0

Functions (5)

$Y_0 =$

$\vdots \quad \vdots$

$R_{3Out} =$

} for H/W.

Design of logic (6)

also using gated D latches.

Final exam